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OFGS File No.	:	P/1071-537
Inventor	:	Yasushi UENO, et al.
Title	:	LAMINATED CERAMIC ELECTRONIC PARTS
Assignee	:	Murata Manufacturing Co., Ltd.

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

12 Pages of Specification including Abstract and Claims
1 Numbered Claims Calculated as 1 Claims for Fee Purposes
1 Sheets of Drawing Containing Figures 1 to 2. (Informal)
X Declaration and Power of Attorney (Unexecuted)
X Priority is Claimed under 35 U.S.C. §119:
Convention Date May 9, 1997 for Japanese Appln. S.N. 9-135823
____ Certified Priority Application
____ Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.
____ Assignment
X Return-Addressed Post Card

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Name of Person Mailing Correspondence

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LAMINATED CERAMIC ELECTRONIC PARTS

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to laminated ceramic electronic parts and more specifically to laminated ceramic electronic parts such as a laminated ceramic capacitor and a laminated varistor having a structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within a ceramic element composing the electronic part.

Description of Related Art:

A surface mounted laminated ceramic capacitor which is one of typical laminated ceramic electronic parts is constructed by disposing external electrodes 24a and 24b which electrically conduct with a plurality of internal electrodes 22 at both ends of a ceramic element (capacitor element) 23 having a structure in which the internal electrodes 22 are disposed so as to face each other via ceramic layers 21a within dielectric ceramic 21 and respective one ends of the internal electrodes 22 are led alternately to the opposite side as shown in FIG. 2 and is characterized in that it can obtain a large capacitance even though it is small.

By the way, with the miniaturization and the enhancement of capacity of the laminated electronic parts, the ceramic layer 21a within the laminated ceramic electronic parts such as the laminated ceramic capacitor have come to be thinned and a number of laminated layers thereof to be increased rapidly and those having a structure in which a thickness of the ceramic layer 21a

interposed between the internal electrodes 22 (effective thickness of element) is 5 μm and the number of lamination exceeds 100 have come to be put on the market.

The ceramic layer 21a has come to be thinned such that there is no big difference with the thickness of the internal electrode 22 in such laminated ceramic electronic parts and even one in which a rate of a total thickness of respective internal electrodes to a thickness of a ceramic element (chip) (thickness of internal electrodes (total)/thickness of ceramic layer) exceeds 0.30 has come to be provided.

Then, thereby, a sintering characteristic of the laminated ceramic electronic part, i.e. the product, is largely influenced by a sintering characteristic of a material of the internal electrode in a sintering process. As a result, there has been a problem that when the rate of the material of the internal electrode to the ceramic element increases, an incidence of delamination and crack increases in the sintering process, thus increasing a fraction defective and degrading the reliability. Further, such laminated ceramic electronic part has had a problem that it is liable to cause cracks when it receives a thermal shock.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to solve the above-mentioned problems by providing highly reliable laminated ceramic electronic parts in which delamination or crack can be suppressed from occurring during a sintering process and which excels in thermal shock resistance even if a number of lamination of internal electrodes is increased and a thickness of a ceramic layer is reduced.

In order to achieve the above-mentioned object, the inventive laminated ceramic electronic part having a structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within a ceramic element and the internal electrodes are led to terminals on the opposite side of the ceramic element per layer is characterized in that it satisfies the following requirements:

(a) a thickness of the ceramic layer is 10 μm or less;

(b) a number of lamination of the internal electrodes is 200 or more;

(c) a ratio of the thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and

(d) a ratio (volume of internal electrode/volume of ceramic element) of a volume of the internal electrode to a volume of the ceramic element (total volume of internal electrodes and the ceramic) is 0.10 to 0.30.

It becomes possible to suppress delamination and crack from occurring during the sintering process, to improve the thermal shock resistance and to provide the highly reliable laminated ceramic electronic part even when the number of lamination of the internal electrodes is increased and the thickness of the ceramic layer is reduced by satisfying the requirements of that the thickness of the ceramic layer is 10 μm or less; the number of lamination of the internal electrodes is 200 or more; the ratio of the thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and the ratio of the volume of the internal electrodes to the volume of the ceramic element

(volume of internal electrodes/volume of ceramic element) is 0.10 to 0.30.

That is, it becomes possible to suppress the influence of the sintering characteristic of the material of the internal electrode during the sintering process and to prevent delamination and crack from occurring during the sintering by controlling the ratio of the thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) and it becomes possible to enhance the strength of the laminated ceramic electronic part against thermal stress and to provide the highly reliable laminated ceramic electronic part by controlling the ratio (volume of internal electrodes/volume of ceramic element) of the volume of the internal electrodes to the volume of the ceramic element (total volume of internal electrodes and the ceramic).

The specific nature of the invention, as well as other objects, uses and advantages thereof, will clearly appear from the following description and the from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING(S)

FIG. 1 is a section view showing a structure of a laminated ceramic electronic part (laminated ceramic capacitor) according to one embodiment of the present invention; and

FIG. 2 is a section view showing a structure of a prior art laminated ceramic electronic part (laminated ceramic capacitor).

DESCRIPTION OF PREFERRED EMBODIMENT

One preferred embodiment of the present invention will

be described below in detail. FIG. 1 is a section view showing a structure of a laminated ceramic electronic part (laminated ceramic capacitor in the present embodiment) according to the embodiment of the invention.

As shown in FIG. 1, the laminated ceramic capacitor is constructed by disposing external electrodes 4a and 4b which electrically conduct with a plurality of internal electrodes 2 at both ends of a ceramic element (capacitor element) 3 having a structure in which the internal electrodes 2 are disposed so as to face each other via ceramic layers 1a within ceramic 1 and respective one ends of the internal electrodes 2 are led to the opposite side alternately.

It is noted that in fabricating such a laminated ceramic capacitor, three kinds of green sheets whose thickness turn out to be 9.8 μm, 6.2 μm and 4.3 μm, respectively, after sintering have been formed. Then, conductive paste for forming the internal electrode has been printed on one surface of the green sheets such that they turn out to have thickness as shown in Table 1. Then, after laminating and compressing them such that a number of lamination of the internal electrodes turns out to be 200, they have been cut into a predetermined size (length L = 3.2 mm, width W = 1.6 mm) to obtain laminates (non-sintered ceramic element).

Next, after treating the laminate by heat to degrease and to sinter under predetermined conditions, conductive paste for forming the external electrode has been applied on the both ends of the sintered ceramic element. Then, they have been sintered to form the external electrodes and the laminated ceramic capacitor as shown in FIG. 1 has been obtained.

Then, characteristics of each laminated ceramic

capacitor thus obtained, such as a value of electrostatic capacity to be obtained, a value of insulation resistance, an incidence of delamination and an incidence of crack on the surface of the ceramic element as well as an incidence of crack (incidence of thermal shock crack) when a thermal shock (_T = 350°C) is applied have been studied. Table 1 shows the result.

TABLE 1

	Thickness of Ceramic Light	Thickness of Internal Electrode	Ratio of Thickness of Internal Electrode	Ratio of Volume of Internal Electrode	Value of Electrostatic Capacity	Value of Insulation Resistance	Incidence of Delamination	Incidence of Crack	Incidence of Thermal Shock Crack
	(μm)	(μm)	(-)	(-)	(μF)	log IR	(%)	(%)	(%)
* 1	9.8	0.68	0.06	0.075	1.81	12.01	0.00	0.00	0.00
2	9.8	0.99	0.10	0.100	2.25	12.00	0.00	0.00	0.00
3	9.8	1.13	0.15	0.112	2.37	11.98	0.00	0.00	0.00
4	9.8	1.97	0.20	0.186	2.43	11.87	0.00	0.00	0.00
* 5	9.8	2.50	0.26	0.307	2.23	11.98	0.33	1.35	2.13
* 6	6.2	0.58	0.09	0.095	2.78	11.53	0.00	0.00	0.00
7	6.2	0.87	0.14	0.135	3.54	11.25	0.00	0.00	0.00
8	6.2	1.15	0.19	0.172	3.42	11.15	0.00	0.00	0.00
9	6.2	1.87	0.31	0.257	3.15	11.01	0.00	0.01	0.00
*10	6.2	2.40	0.38	0.310	3.07	11.07	0.53	0.97	0.54
*11	4.3	0.41	0.95	0.103	3.98	10.10	0.00	0.00	0.00
12	4.3	0.71	0.16	0.170	4.54	10.93	0.00	0.00	0.00
13	4.3	0.97	0.23	0.200	4.95	11.25	0.00	0.00	0.00
14	4.3	1.23	0.29	0.210	5.01	10.98	0.00	0.00	0.00
*15	4.3	1.65	0.41	0.310	4.99	10.33	0.13	0.52	1.58
*16	4.3	2.40	0.56	0.390	4.83	10.54	0.97	1.35	3.51

It is noted that in Table 1, those samples marked with * are those out of the scope of the present invention (comparative examples) and the other samples are those within the scope of the invention.

Further, "Rate of Thickness of Internal Electrode" is the rate of the thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) and "Rate of Volume of Internal Electrode" is the rate of the volume of the internal electrodes to the volume of the ceramic layer (total volume of the internal electrodes and the ceramic).

Further, the evaluating items and a number of evaluated samples (n) in Table 1 has had the following relationship:

Electrostatic Capacity, Insulation Resistance : n = 100

Incidence of Delamination and Crack : n = 500

Incidence of Crack due to Thermal Shock : n = 500

As shown in Table 1, it has been confirmed that while (1) the value of electrostatic capacity is small in Sample No. 1 whose rate of the thickness of the internal electrode is below that of the scope of the invention (0.10 to 0.40), (2) the value of insulation resistance is small in Sample No. 11 whose rate of the thickness of the internal electrode exceeds that of the scope of the invention, and (3) the incidences of delamination, crack and crack due to thermal shock are high in Sample Nos. 5, 10, 15 and 16 whose rate of the volume of the internal electrode exceeds that of the scope of the invention (0.10 to 0.30), the samples within the scope of the invention which satisfy the

requirements of that the rate of the thickness of the internal electrode to that of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40 and the rate of the volume of the internal electrode to the volume of the ceramic element (volume of internal electrode/volume of ceramic element) is 0.10 to 0.30 can obtain characteristics which are practically no problem with respect to the values of electrostatic capacity and of insulation resistance, cause no delamination nor crack during the sintering process and cause no crack due to thermal shock.

It is noted that while the present embodiment has been explained by exemplifying the laminated ceramic capacitor, the present invention is applicable not only to the laminated ceramic capacitor but also to various laminated ceramic electronic parts such as a laminated varistor having the structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within the ceramic element.

The present invention is not limited to the embodiment described above also in other points. That is, it is possible to add various applications and modifications thereto within the scope of the invention with respect to the thickness of the ceramic layer, the number of lamination of the internal electrodes, the rate of the thickness of the internal electrode to that of the ceramic layer, the rate of the volume of the internal electrode to that of the ceramic element and the like.

As described above, because the inventive laminated ceramic electronic part is constructed so as to satisfy the requirements of that the thickness of the ceramic layer is 10 μm or less; the number of lamination of the internal electrodes is 200 or more; the ratio of the thickness of

the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and the ratio of the volume of the internal electrode to the volume of the ceramic element is 0.10 to 0.30, it is possible to suppress the influence of the sintering characteristic of the material of the internal electrode during the sintering process, to prevent delamination and crack from occurring during the sintering and to enhance the strength of the laminated ceramic electronic part against thermal stress.

As a result, it becomes possible to suppress delamination and crack from occurring during the sintering process even when the number of lamination of the internal electrodes is increased and the thickness of the ceramic layer is reduced and to provide the highly reliable laminated ceramic electronic part which excels in the thermal shock resistance.

While the preferred embodiment has been described, variations thereto will occur to those skilled in the art within the scope of the present inventive concept which is delineated by the following claim.

WHAT IS CLAIMED IS:

1. A laminated ceramic electronic part having a structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within a ceramic element and said internal electrodes are led to terminals on the opposite side of said ceramic element per layer;

said laminated ceramic electronic part being characterized in that it satisfies the following requirements:

(a) a thickness of said ceramic layer is 10 μm or less;

(b) a number of lamination of said internal electrodes is 200 or more;

(c) a ratio of the thickness of said internal electrode to the thickness of said ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and

(d) a ratio (volume of internal electrodes/volume of ceramic element) of a volume of said internal electrode to a volume of said ceramic element (total volume of internal electrodes and ceramic) is 0.10 to 0.30.

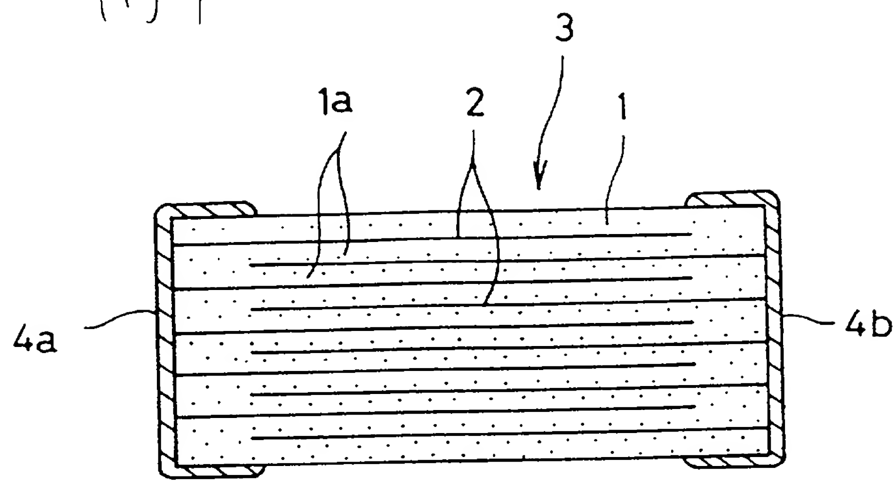
LAMINATED CERAMIC ELECTRONIC PARTS

ABSTRACT OF THE DISCLOSURE

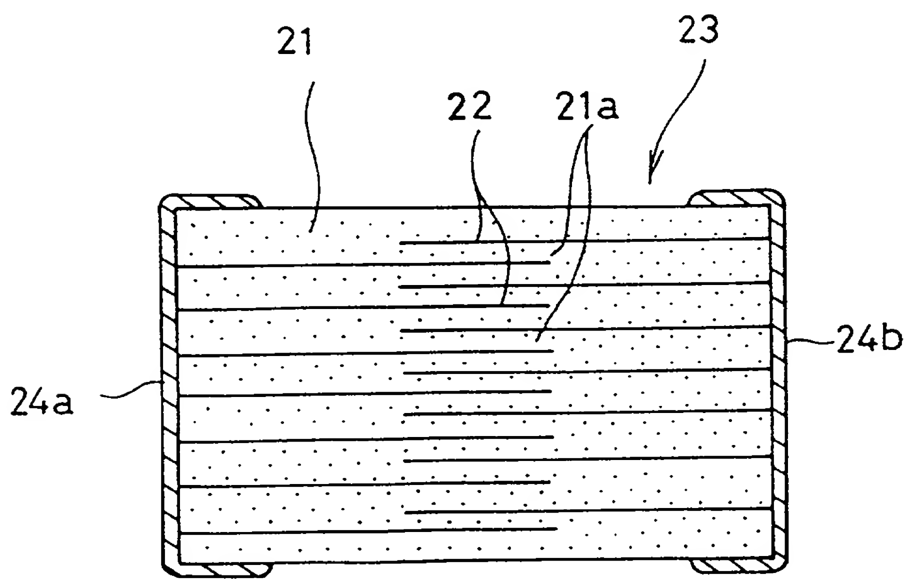
There is provided a highly reliable laminated ceramic electronic part in which delamination or crack can be suppressed from occurring during a sintering process even if a number of lamination of internal electrodes is increased and a thickness of the ceramic layer is reduced and which excels in thermal shock resistance. The laminated ceramic electronic part is constructed so as to satisfy the following requirements of that a thickness of the ceramic layer is 10 μm or less; a number of lamination of the internal electrodes is 200 or more; a ratio of a thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and a ratio of a volume of the internal electrode to a volume of the ceramic element (volume of internal electrodes/volume of ceramic element) is 0.10 to 0.30.

【書類名】図面

【図１】 Fig. 1



【図２】 Fig. 2



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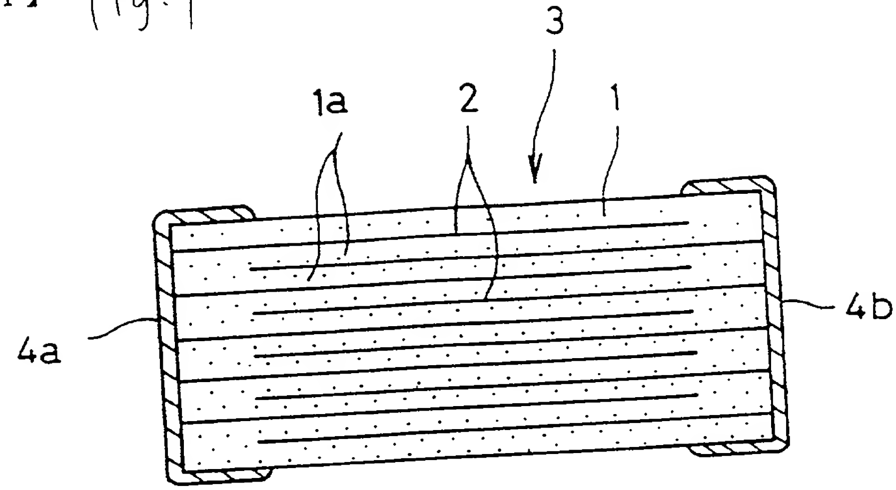
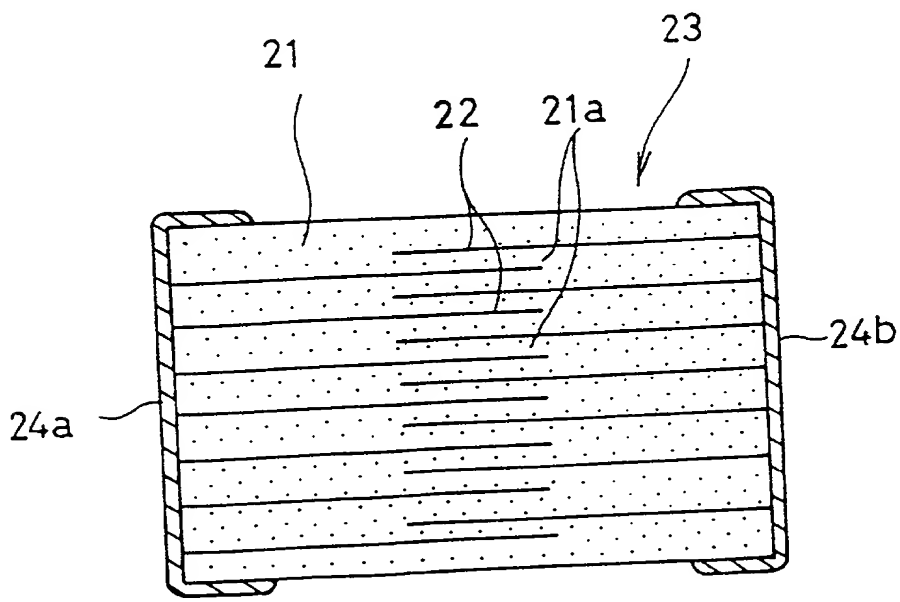
【書類名】図面

【図１】 Fig. 1



【図２】 Fig. 2



UNITED STATES OF AMERICA COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION	OFGS FILE NO. P/1071-537

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LAMINATED CERAMIC ELECTRONIC PARTS

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on ______________ as United States patent Application Number or PCT International patent application number ______________ and was amended on ______________ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	9-135823	09 May 1997	YES X NO ___
			YES ___ NO ___
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I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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COUNTRY	APPLICATION NUMBER	DATE OF FILING *(day, month, year)*	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES ___ NO ___
			YES ___ NO ___
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			YES ___ NO ___

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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